**AMENDMENTS TO THE CLAIMS**:

1. (Currently Amended) A digital-to-analog converter for converting a digital signal to an analog signal comprising:

a modulator for applying Delta-Sigma modulation to the digital signal to generate a code sequence;

a first post-filter having a first-order attenuation characteristic of performing low-pass filtering to the code sequence; and

a second post-filter having another first-order attenuation characteristic of performing low-pass filtering to an output signal from said first post-filter, and for outputting the processed analog signal;

~~wherein said first and second post-filters have different cutoff frequencies~~

wherein a cutoff frequency of said first post-filter is set in a frequency range between a cutoff frequency of said second post-filter and a maximum frequency at which the attenuation of said second post-filter reaches a predetermined value of attenuation, in order to simultaneously execute processing such as de-emphasis in a frequency range between said cutoff frequency of said second post-filter and said first post-filter, and elimination of high-frequency noise over said cutoff frequency of said first post-filter.

2. (Canceled)

3. (Currently Amended) The digital-to-analog converter according to claim [[2]] 1, wherein the cutoff frequency of said first post-filter is set in a frequency range of 20 to 30kHz, and the cutoff frequency of said second post-filter is set in a frequency range of 2 to 3 kHz.

4. (Original) The digital-to-analog converter according to claim 1, wherein each of said first and second post-filters is a first-order analog low-pass filter composed of a resistor and a capacitor.

5. (Original) The digital-to-analog converter according to claim 4, wherein said resistor composing said first post-filter is connected to an output of said modulator and is fabricated in a semiconductor integrated circuit device together with said modulator.

6. (Original) The digital-to-analog converter according to claim 1, further comprising:

an impedance converter connected to a subsequent stage of said second post-filter, to convert impedance of the analog signal being output from said second post-filter.

7. (Original) The digital-to-analog converter according to claim 6, further comprising:

voltage dividing resistors for dividing a voltage of the analog signal being output from said impedance converter.

8. (Original) The digital-to-analog converter according to claim 5, wherein said semiconductor integrated circuit device is provided with an FM receiving section placed at a preceding stage of said modulator.

9. (Original) The digital-to-analog converter according to claim 8, wherein said FM receiving section comprises an RF amplifier, a frequency converter, an A/D converter, a frequency discriminator and a matrix circuit to generate a detected signal from a received signal.

10. (New) A digital-to-analog converter for converting a digital signal to an analog signal comprising:

a modulator for applying Delta-Sigma modulation to the digital signal to generate a code sequence;

a first post-filter having a first-order attenuation characteristic of performing low-pass filtering to the code sequence;

a second post-filter having another first-order attenuation characteristic of performing low-pass filtering to an output signal from said first post-filter, and for outputting the processed analog signal;

an impedance converter connected to a subsequent stage of said second post-filter, to convert impedance of the analog signal being output from said second post-filter; and

voltage dividing resistors for dividing a voltage of the analog signal being output from said impedance converter, wherein

said first and second post-filters have different cutoff frequencies.

11. (New) A digital-to-analog converter for converting a digital signal to an analog signal comprising:

a modulator for applying Delta-Sigma modulation to the digital signal to generate a code sequence;

a first post-filter having a first-order attenuation characteristic of performing low-pass filtering to the code sequence; and

a second post-filter having another first-order attenuation characteristic of performing low-pass filtering to an output signal from said first post-filter, and for outputting the processed analog signal,

wherein said first and second post-filters have different cutoff frequencies,

wherein each of said first and second post-filters is a first-order analog low-pass filter composed of a resistor and a capacitor,

wherein said resistor composing said first post-filter is connected to an output of said modulator and is fabricated in a semiconductor integrated circuit device together with said modulator,

wherein said semiconductor integrated circuit device is provided with an FM receiving section placed at a preceding stage of said modulator, and

wherein said FM receiving section comprises an RF amplifier, a frequency converter, an A/D converter, a frequency discriminator and a matrix circuit to generate a detected signal from a received signal.